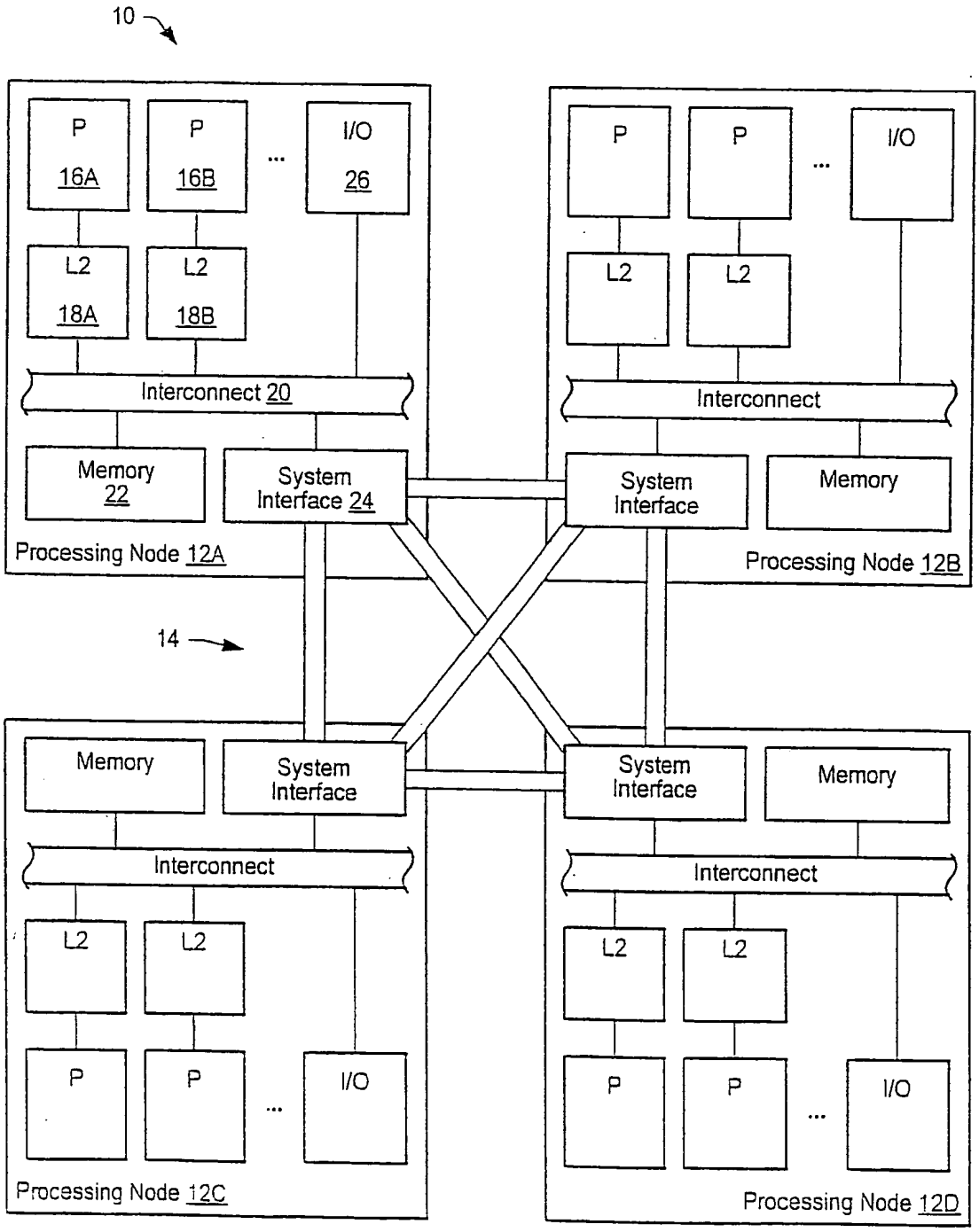
10
P
16A
P
16B
I/O
26
L2
18A
L2
18B
Interconnect 20
Memory
22
System
Interface 24
Processing Node 12A
P
P
I/O
L2
L2
Interconnect
System
Interface
Memory
Processing Node 12B
14
Memory
System
Interface
Interconnect
L2
L2
P
P
I/O
Processing Node 12C
System
Interface
Memory
Interconnect
L2
L2
P
P
I/O
Processing Node 12D

Fig. 1

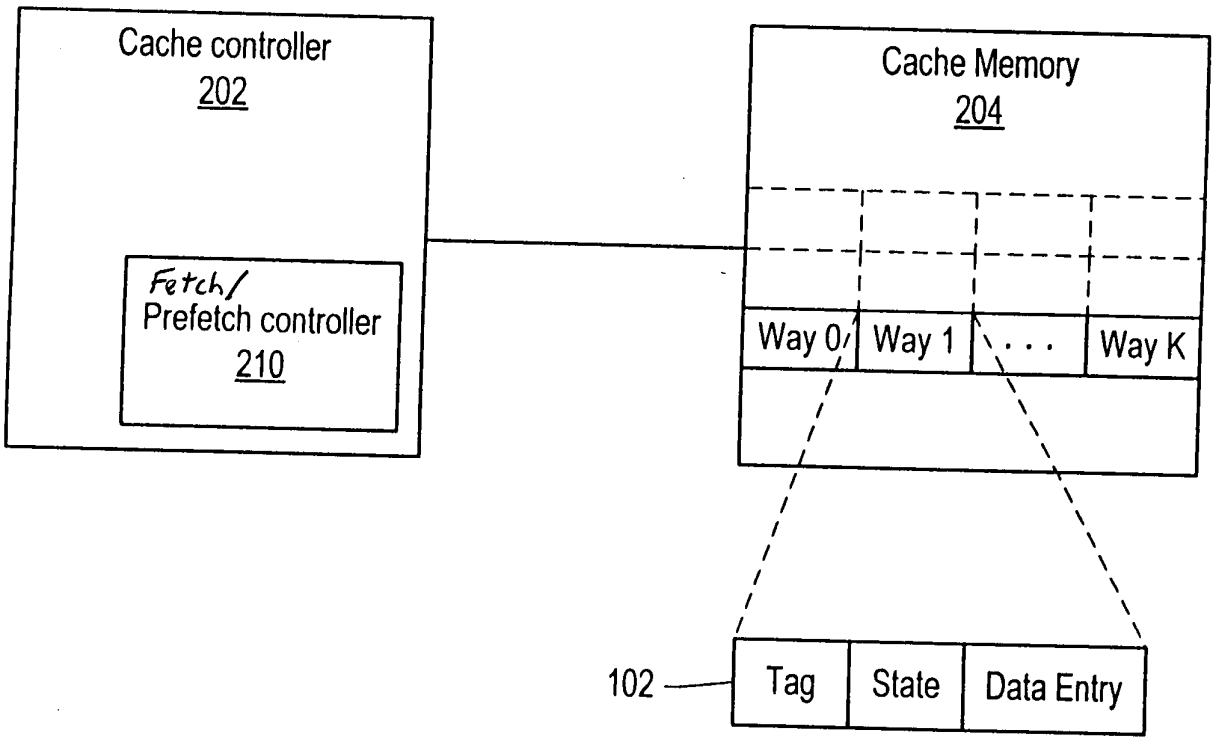
Cache controller
202
Fetch/
Prefetch controller
210
Cache Memory
204
Way 0
Way 1
. . .
Way K
102
Tag
State
Data Entry

FIG. 2

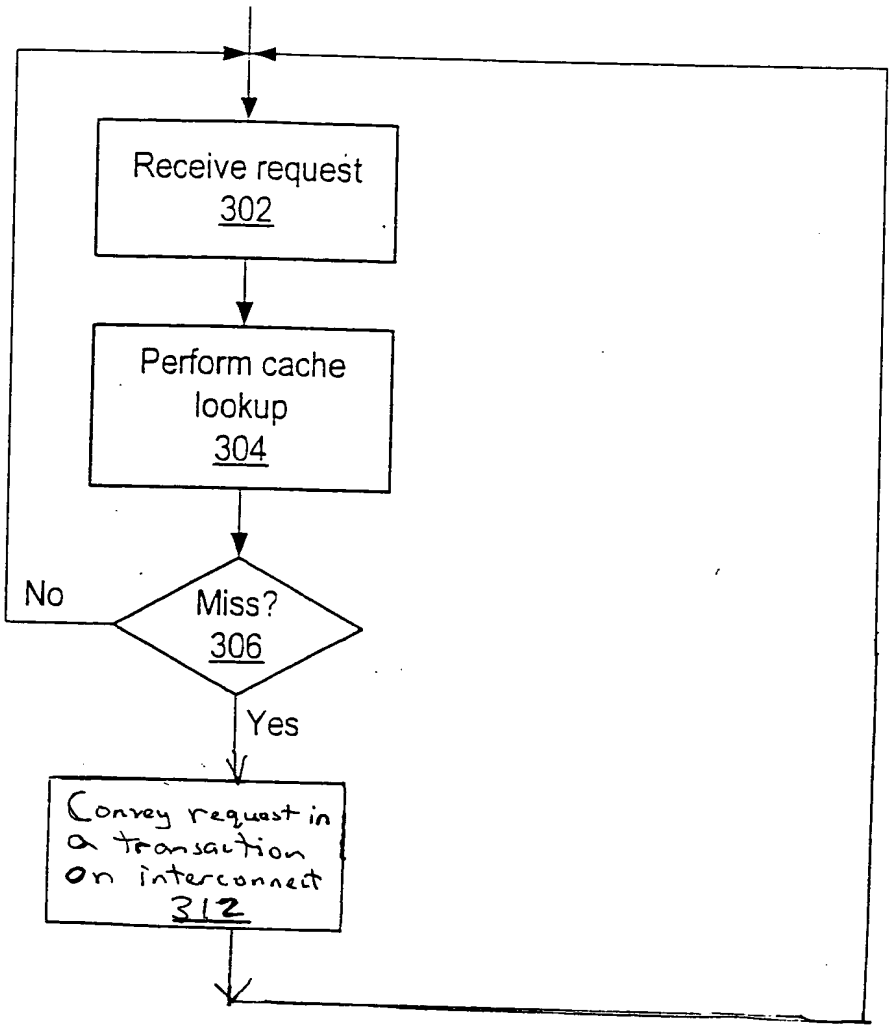

Fig. 3

Request Type	Prefetch Bit Map	Address

FIG. 4

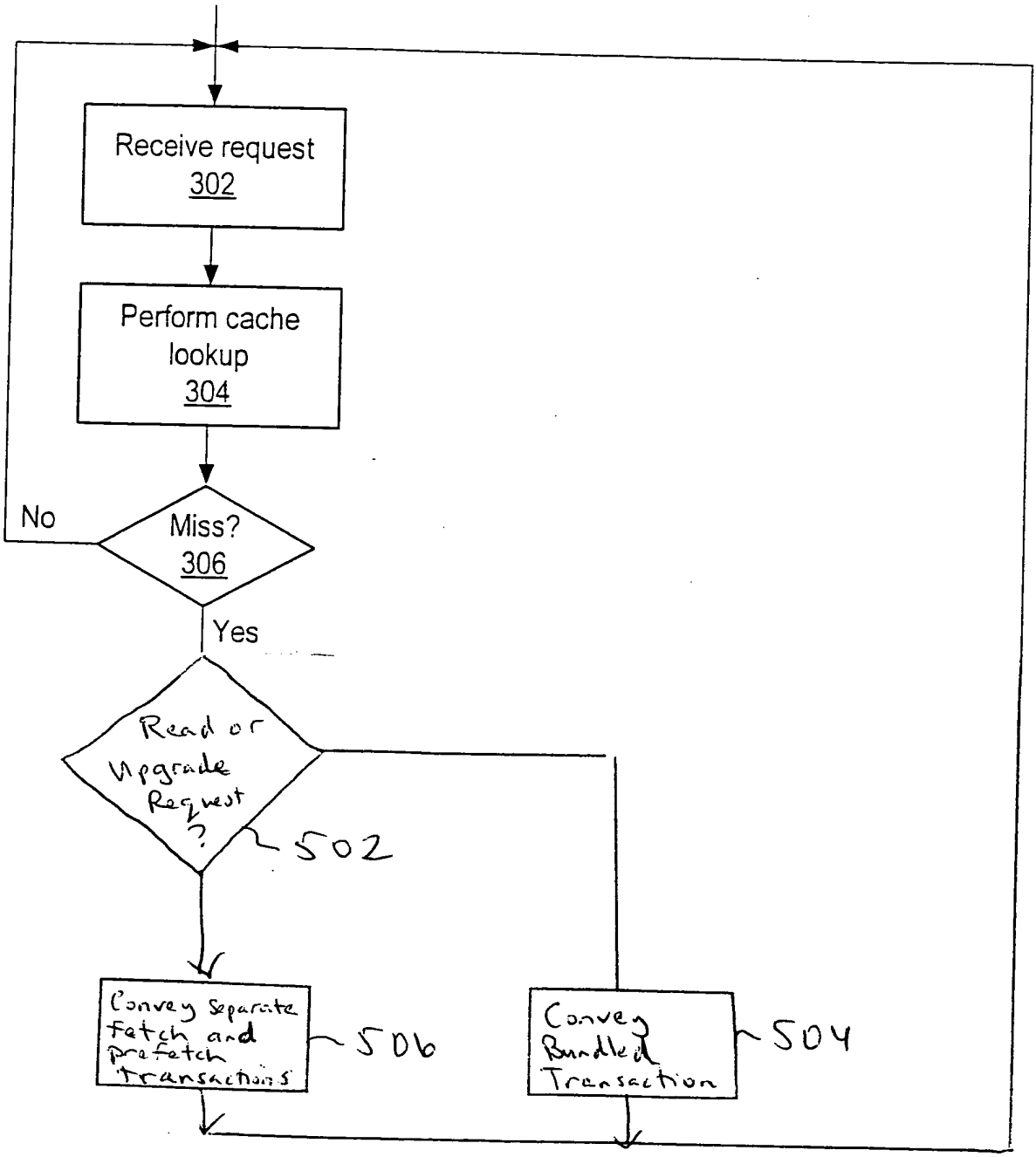
Receive request
302
Perform cache lookup
304
No
Miss?
306
Yes
Read or Upgrade Request ?
502
Convey Separate fetch and prefetch Transactions
506
Convey Bundled Transaction
504

FIG. 5

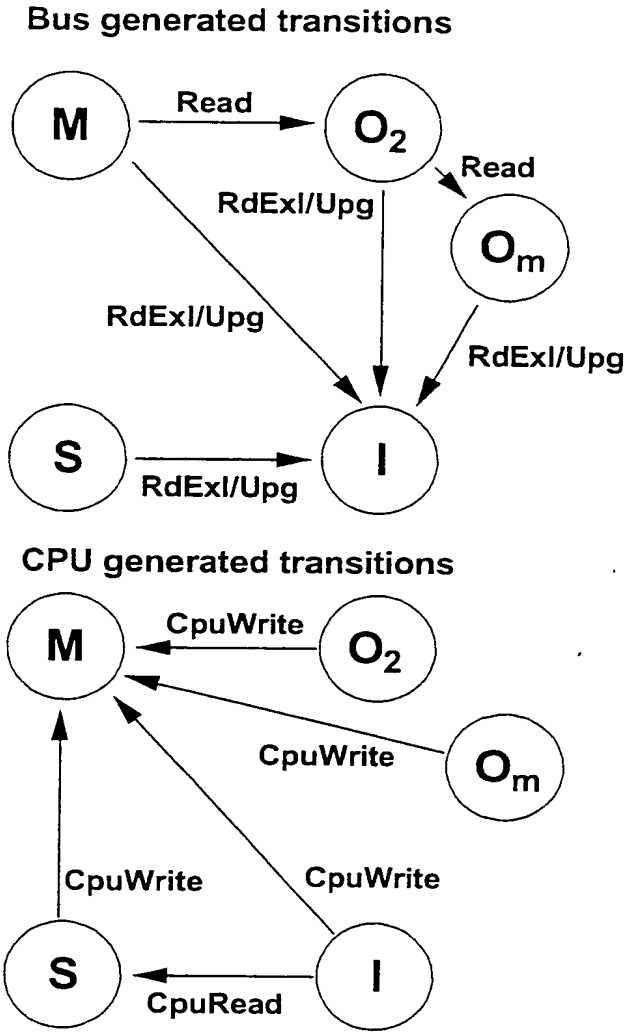
Bus generated transitions
M
Read
O_2
Read
RdExl/Upg
O_m
RdExl/Upg
RdExl/Upg
S
I
RdExl/Upg
CPU generated transitions
M
CpuWrite
O_2
CpuWrite
O_m
CpuWrite
CpuWrite
S
I
CpuRead

Fig. 6

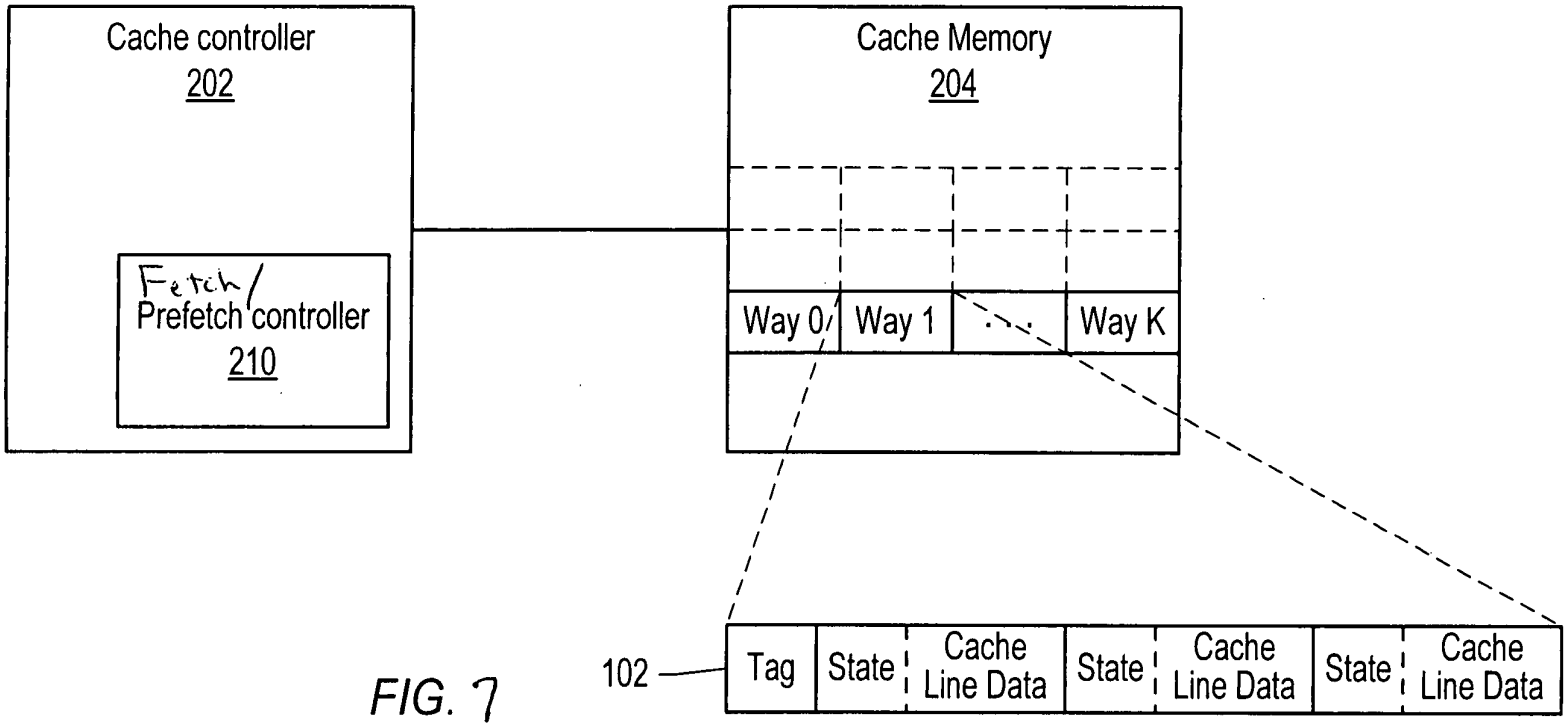
Cache controller
202
Fetch/
Prefetch controller
210
Cache Memory
204
Way 0
Way 1
Way K
102
Tag
State
Cache Line Data
State
Cache Line Data
State
Cache Line Data

FIG. 7